# 2021x Version News
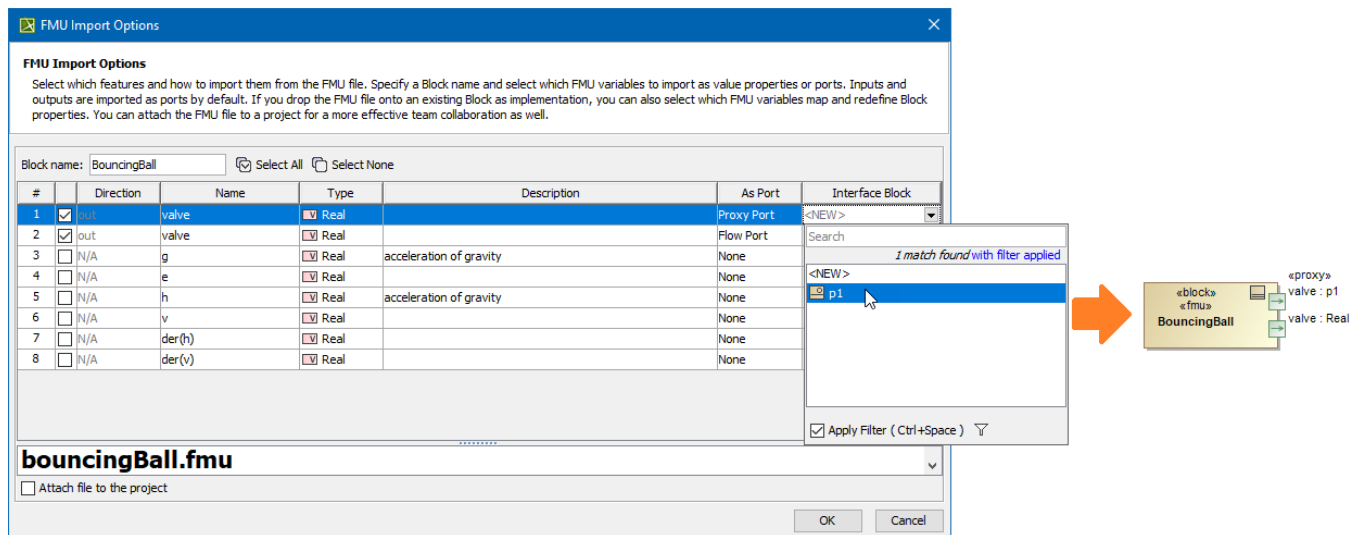
The 2021x release is packed with a few improvements that extended the usage of Simulink import and Modelica export. We introduce the new SysML 1.6 specification support, including new concepts such as Conjugated Interface Block, «AddFlowPropertyValueOnNestedPortAction» stereotype, additional Binding Connector notation, renamed compartments, enumerations, and more.

Download it today at nomagic.com or contact your sales representative, and don't forget to give us your feedback on Twitter or Facebook.

- Proxy Ports in FMU and Simulink import
- Simulink model import to Activities
- Simulink composite signals export
- IBD-based selective Modelica export
- SysML 1.6 support
- Key Issues Fixed

## Proxy Ports in FMU and Simulink import

FMU and Simulink import now support Proxy Port creation. Once you have imported the external FMU/Simulink model, you can select the Proxy Port to be created in your model and then specify an existing or create a new Interface Block to be used as its type.
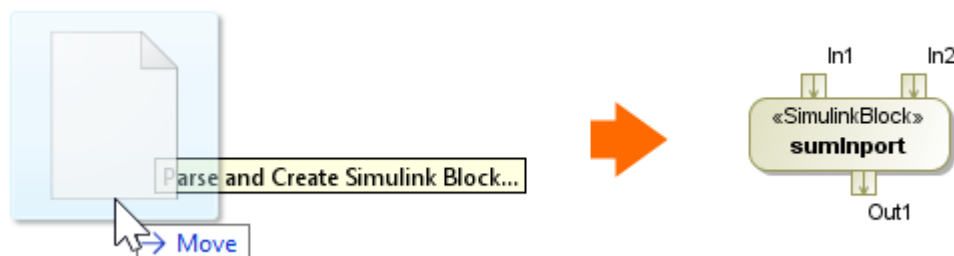


Selecting the Proxy Port and an Interface Block upon the external model import.

Learn more about FMU and Simulink import >>

## Simulink model import to Activities

You can import the Simulink model by dragging and dropping the Simulink file (*.slx) directly onto the Activity diagram. The Activity (stereotyped by «SimulinkBlock») which is assigned as behavior for the Call Behavior Action and its Input and/or Output Pins are created in the model.
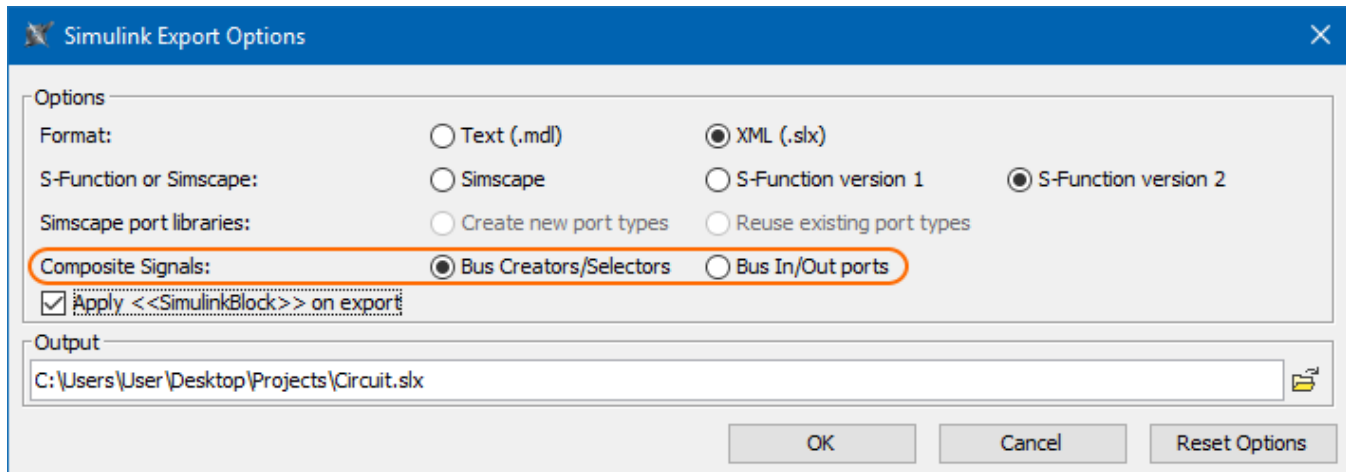
Learn more about Simulink import >>

## Simulink composite signals export

**You can now select how to export** Proxy Port or Interface Block with multiple Flow Properties (composite signals): as bus Creators/Selectors or as bus In /Out ports.



Learn more about Simulink export  >>

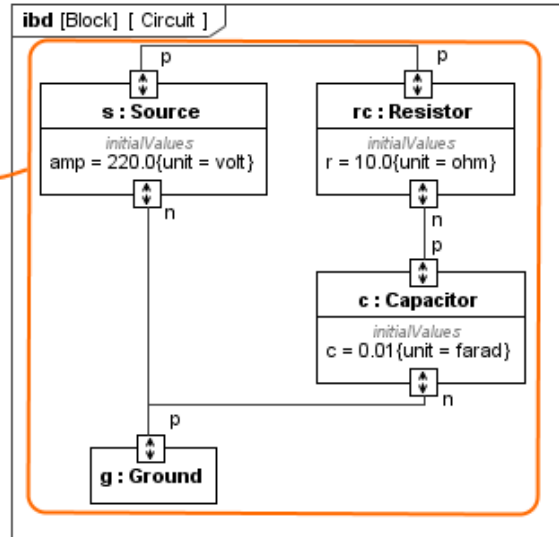## IBD-based selective Modelica export

You can now use the Internal Block Diagram to select what to export to Modelica. Only parts, ports, and connectors appearing in this diagram are exported, rather than the entire model. See whole vs partial export comparison in the image below.

## IBD exported to Modelica

```
model Circuit
  Circuit _Circuit;
  model Circuit
    Source s(amp.start=220.0,amp.fixed=true);
    Capacitor c(c.start=0.01,c.fixed=true);
    Ground g;
    Resistor rc(r.start=10.0,r.fixed=true);
  equation
    connect(g.p,s.n);
    connect(s.p,rc.p);
    connect(c.p,rc.n);
    connect(c.n,s.n);
  end Circuit;
```

**ibd** [Block] [ Circuit ]

```
        p                          p
   ┌────┴────┐              ┌──────┴──────┐
   │ s : Source │          │ rc : Resistor │
   │ initialValues │       │ initialValues │
   │ amp = 220.0{unit = volt} │   r = 10.0{unit = ohm} │
   └────┬────┘              └──────┬──────┘
        n                          n
                                   p
                            ┌──────┴──────┐
                            │ c : Capacitor │
                            │ initialValues │
                            │ c = 0.01{unit = farad} │
                            └──────┬──────┘
                                   n
        p
   ┌────┴────┐
   │ g : Ground │
   └─────────┘
```
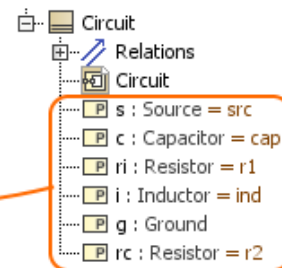
## Block exported to Modelica

```
model Circuit_full
  Circuit _Circuit_full;
  model Circuit
    Source s(amp.start=220.0,amp.fixed=true);
    Capacitor c(c.start=0.01,c.fixed=true);
    Resistor ri(r.start=20.0,r.fixed=true);
    Inductor i(l.start=0.1,l.fixed=true);
    Ground g;
    Resistor rc(r.start=10.0,r.fixed=true);
  equation
    connect(g.p,s.n);
    connect(s.p,rc.p);
    connect(rc.p,ri.p);
    connect(ri.n,i.p);
    connect(i.n,c.n);
    connect(c.p,rc.n);
    connect(c.n,s.n);
  end Circuit;
```

- Circuit
  - Relations
  - Circuit
    - s : Source = src
    - c : Capacitor = cap
    - ri : Resistor = r1
    - i : Inductor = ind
    - g : Ground
    - rc : Resistor = r2

The difference between whole (exporting Block) and partial (exporting IBD) export to the Modelica file.

Learn more about Modelica export >>

## SysML 1.6 support

As of version 2021x the SysML Plugin supports the SysML 1.6 specification which brings the following improvements:

- One more way to model conjugated ports is to create the Conjugated Interface Block which has the same features as its original Interface Block except that its Directed Features and Flow Properties are reversed (conjugated). Learn more about Conjugated Interface Block >>
- The ability to change the Binding Connector notation keyword from "equal" to sign "=". Learn how to create Binding Connector >>
- The new stereotype «AddFlowPropertyValueOnNestedPortAction» is created which enables values added to a flow property to propagate out through a specified behavioral port of an object executing the action, rather than all behavior ports exposing the flow property. It also enables values added to a flow property to propagate into objects.
- The AdjunctProperty principal type is changed from Element to NamedElement.
- The «PropertySpecificType» stereotype is renamed to «pst».
- The Value Type compartment *attributes* is renamed to *properties*.

- The *initialValue* compartment is renamed to *initial values*.
- The s*ignal receptions* compartment is renamed to *receptions*.
- The *FlowDirection, FeatureDirection and ControlValue* enumerations are renamed to *FlowDirectionKind*, *FeatureDirectionKind* and *ControlValueKi nd* respectively.

Learn more about SysML 1.6 support >>

## Key Issues Fixed

The following key issues have been fixed with this version:

- The «SimulinkBlock» references now to Simscape components.
- Initial Values are now exported to Modelica and are recognized by their name and initial values set.
- The Modelica model file starts with a package definition.
- From now on, the *RequirementDerivedPropertyValueUpdater.isTransient()* returns the *true* value for **DerivedFrom** tag.
- The validation now checks if the types of connected ports are different (e.g. *Real* and *String*) and informs about incompatible Flow Properties.
- The **Structure** option is set by default in the Row Query of the SysML Allocation Matrix.